AMENDMENTS IN THE SPECIFICATION

*Please replace paragraph number **[0011]** line 5 beginning on page 4, with the following:*

Because of the latency involved in providing data on the data bus following a DMA Claim and/or a DClaim operation, current systems typically send these operations out on the address bus ahead of time to reserve the cache line and trigger the movement of most coherent data to the device's cache from another cache, if required. However, the data sent to the device cache is typically not needed since the DMA Writes and DCBZ operations overwrite the content of the cache line. Nonetheless, with the MESI protocol, maintaining coherency requires this sequence of address operation followed by data operation to be followed. While the data is being transferred, no other device, is allowed access to the cache line and the device writing to the line has to wait until the data arrives before it can complete the write operation. Thus, significant latency is built into this process. Additionally, placing the data on the data bus for cache-to-cache transfer utilizes a substantial amount of bus resources that could be allocated to other processes.

*Please replace paragraph number **[0038]** line 8 beginning on page 12, with the following:*

In the illustrative embodiment, the MESI protocol is expanded to include a fifth coherency state, which is only assigned when a master device issues a speculative operation for a complete overwrite of the cache line in the device's cache. The new coherency state is referred to herein as the Modified-invalid (Mi) coherency state. Although referred to as Modified-invalid, the Mi state is not a transient state. Rather, the Mi state is a unique state that is recorded within the coherency registers by the directory update logic. A cache line in the master device's cache is tagged with the Mi state following a speculatively issued write operation that initiates a DMA Claim (or D Claim) in the cache hierarchy to secure sole ownership of the [[ache]] cache line for the master device.